Using Decoupling Capacitors

Introduction

This application note describes a number of revised recommendations regarding the use of decoupling capacitors. Network analysis is used to prove that the "conventional" recommendation of using widely spaced values can, in many circumstances, cause less than ideal operation. Simpler, more reliable designs will often result from following the design guidelines of this note.

The Problem

Faster edges, more sensitive devices, and higher clock rates all demand "good" decoupling of the power supplies.

Decoupling:
The art and practice of breaking coupling between portions of systems and circuits to ensure proper operation.

Bypassing:
The practice of adding a low-impedance path to shunt transient energy to ground at the source. Required for proper decoupling.

Design practices that work for lower system speeds and slower logic may not work well when the system speed increases. The common practice of using two different capacitance values for decoupling can:

- Increase the RFI/EMI problems
- Reduce the reliability of operation
- Reduce the noise tolerance

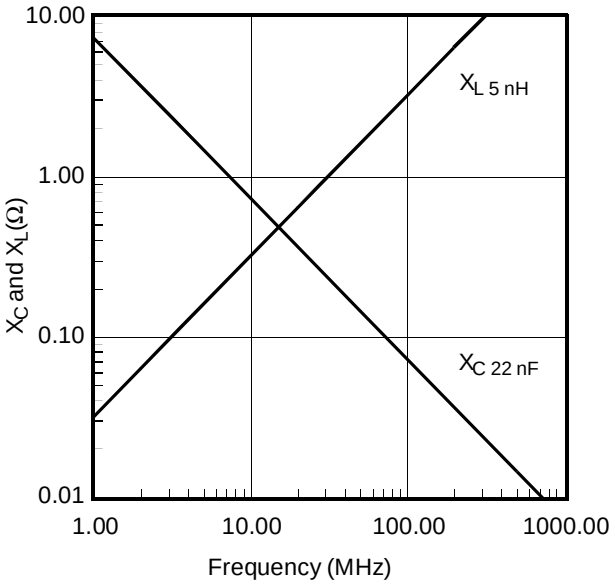

Figure 1. Z vs. f for Parts of a Real Capacitor

Each physical component in a design brings with it additional parasitic components determined by the design and mounting of that component in the system.

Figure 1 shows the behavior of two ideal components, a capacitor and an inductor, which represent the reactive parts of the capacitor shown in *Figure 2*. Note that without any lead inductance or resistance, the resulting capacitive reactance approaches 0Ω with increasing frequency. Note also that the inductive reactance of the ideal inductor, without any stray capacitance, approaches infinity.

A real capacitor includes both an inductor and resistor in the form of leads, traces, and even ground planes in series with it (*Figure 2)*.

Multi-Layer Chip Capacitors (MLC) have approximately 5 nH of parasitic inductance when mounted on a printed circuit board. While the component drawn on the schematic (*Figure 2)* shows a 22-nF capacitor, the system sees the 22-nF capacitor in series with a 5-nH inductor and a 30-mΩ resistor.

The impedance curve of "Real" capacitors resembles the traces marked 22 nF and 100 pF of *Figure 3.* The shape of these calculated curves match those found in a capacitor manufacturer's data sheets. This means that, in a circuit, a capacitor acts as a low-impedance element only over a limited range of frequencies.

To extend this frequency range, many references propose adding a second capacitor to bypass frequencies outside the limited range of the single capacitor. This approach expects a resulting impedance curve like the solid line marked "Expected" in *Figure 3*. This solution, however, is not mathematically sound and has a significant problem at "intermediate" frequencies.

The intermediate frequency problem comes from the parasitic elements present in the "Real" circuit shown in *Figure 4*. The circuit on the left represents the schematic form of a typical decoupling arrangement, a 22-nF and a 100-pF capacitor in parallel.

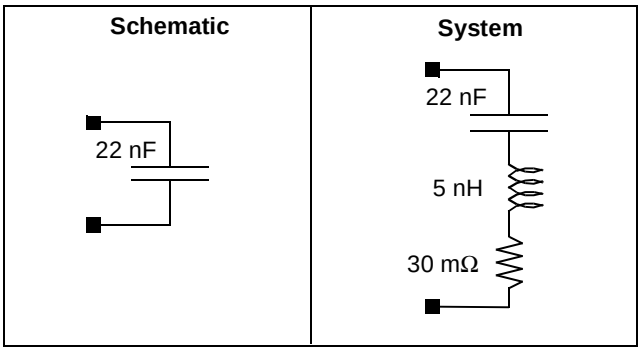

Figure 2. The "Real" Schematic

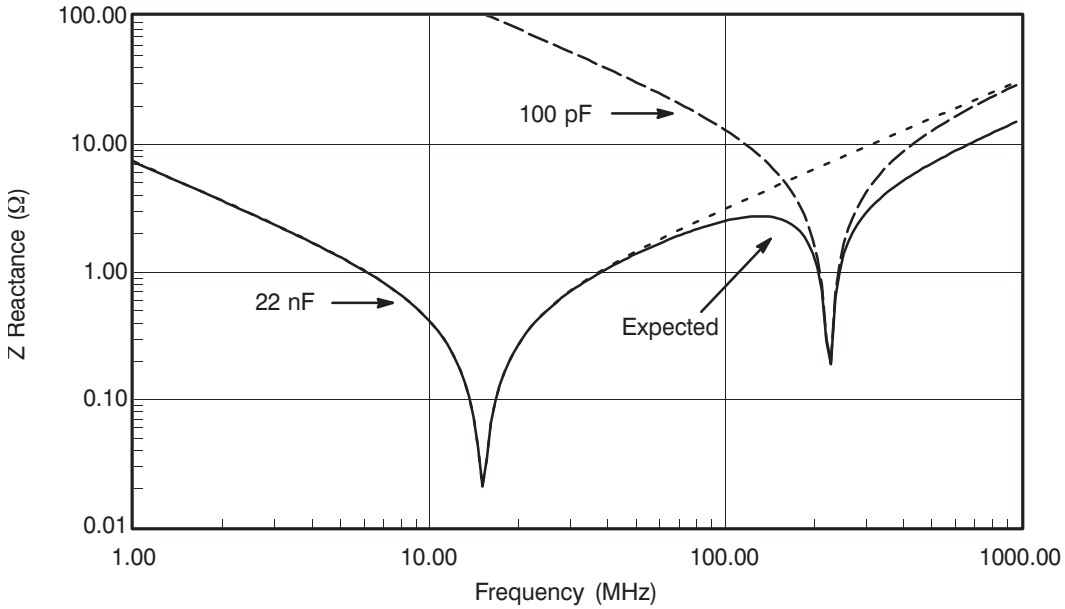

Figure 3. Expected Impedance of "Real" Capacitors

Conventional wisdom suggests that the 100-pF should decouple the high frequencies, and the 22-nF should decouple the low frequencies. However, the combination results in some unexpected interactions. The circuit on the right in *Figure 4* shows a clearer representation of the system, including the parasitic inductances and resistances. It contains all the components necessary to create a resonant tank circuit (with its resulting parallel resonant pole).

Figure 5 shows a combined plot of Z vs. frequency of this circuit. The values given for effective series resistance (ESR; 30 mΩ) and effective series inductance (ESL; 5 nH) are achievable on real PCBs using "good" layouts and surface-mounted capacitors.

The graph of *Figure 5* shows a range of frequencies where this combination of two capacitors results in a higher impedance than that of the larger capacitor alone. For the combination shown, this range includes approximately 15 MHz through 175 MHz. Notice the large peak in reactance at 150 MHz due to parallel resonance of the two capacitors. Any energy from the rest of the system (ICs, clocks, and harmonics), over this intermediate range of frequencies, will see a higher impedance than that of a single 22-nF capacitor alone. Over this range of frequencies, the parallel combination bypasses less of the energy to ground.

The height of the peak shown in *Figure 5* varies inversely with the ESR of the capacitors. As components and board designs improve, the height of the resulting peak actually increases due to a reduction of the system ESR. The exact shape and location of the parallel resonant peak will vary for each system depending on the design of the printed circuit board (PCB) and choice of capacitors.

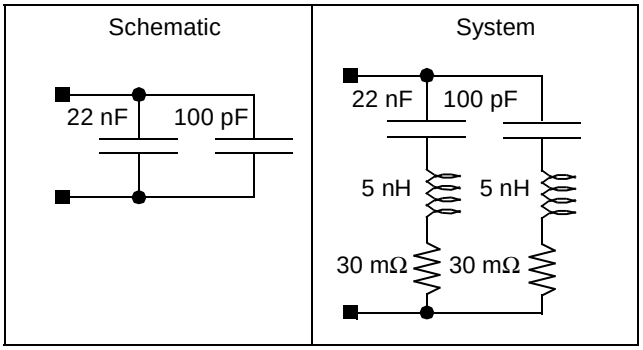

Figure 4. The "Real" Schematic

Recommendations

The following recommendations can improve the resulting designs:

- Use only one value of capacitor.
- Choose the capacitor based on the self-resonant characteristics from the manufacturers' data sheet to match the clock rate or expected noise frequency of the design.
- Use as many capacitors as needed for your range of frequencies. As an example, the capacitor shown (22 nF) has a self resonant frequency of approximately 11 MHz, and a useful (less than 1Ω) impedance range of 6 to 40 MHz. Use as many of these as needed to achieve the desired level of decoupling.
- Use a minimum of one capacitor per power pin, placed as physically close to the to the power pins of the IC as possible to reduce the parasitic inductance.
- Keep lead lengths on the capacitors below 6 mm between the capacitor endcaps and the ground or power pins.
- Place the bypass capacitors on the same side of the PCB as the ICs. *Figure 6* shows an example of a recommended layout for a HOTLink™ Transmitter and Receiver.

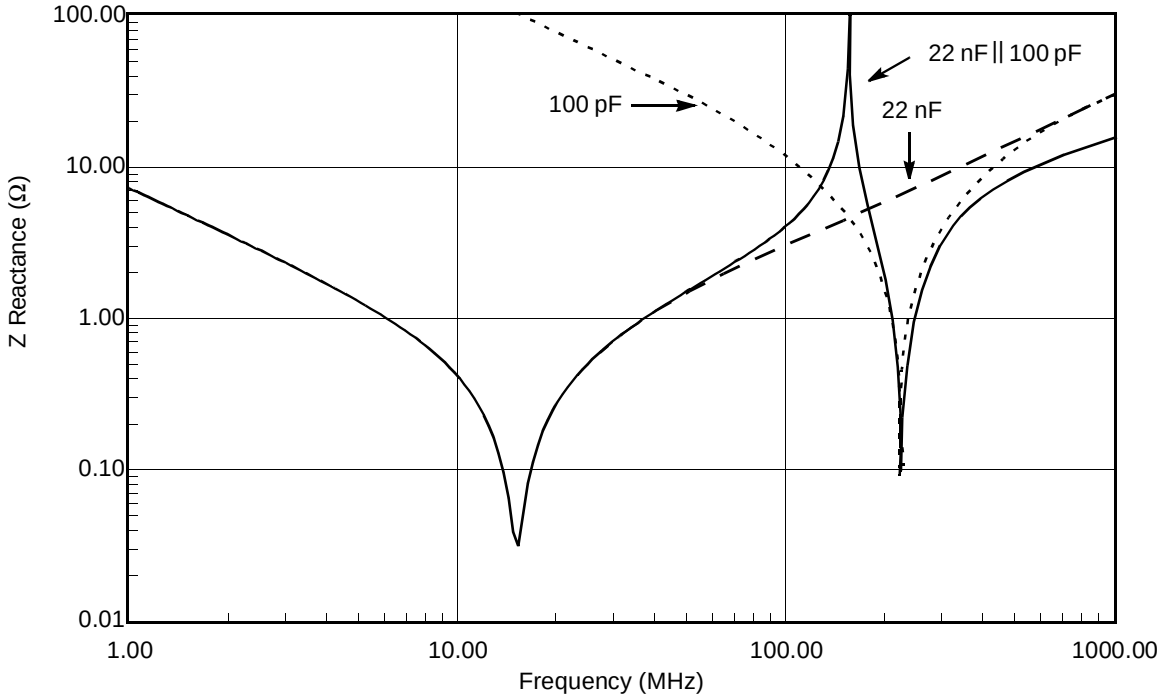

Figure 5. Real Z vs. f for Parallel 22-nF and 100-pF Capacitors

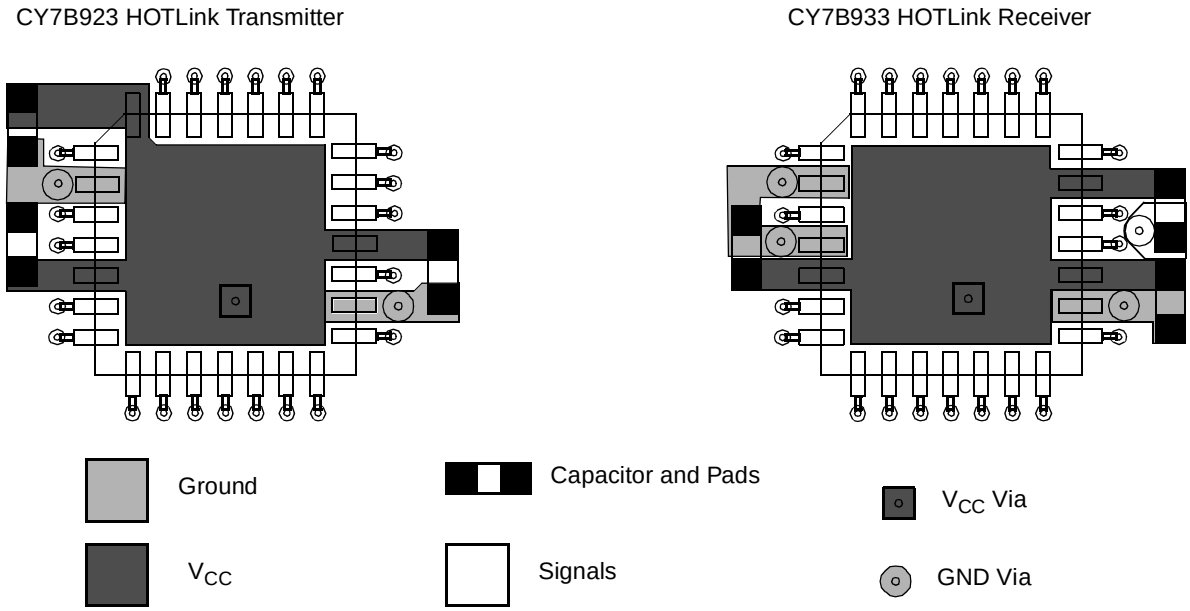

Figure 6. Sample Layouts

A special note about *Figure 6*: in both of the layouts, only one connection is made to the V_{CC} plane. This is done so that the noise, generated both inside the IC and external to this portion of the circuit, must go through the single via to the power plane. The additional reactance of the via helps to keep the noise from spreading throughout the rest of the system.

While HOTLink parts tolerate a fairly large amount of V_{CC} noise, the absolute “best” performance is achieved by following the recommendations listed in this application note.

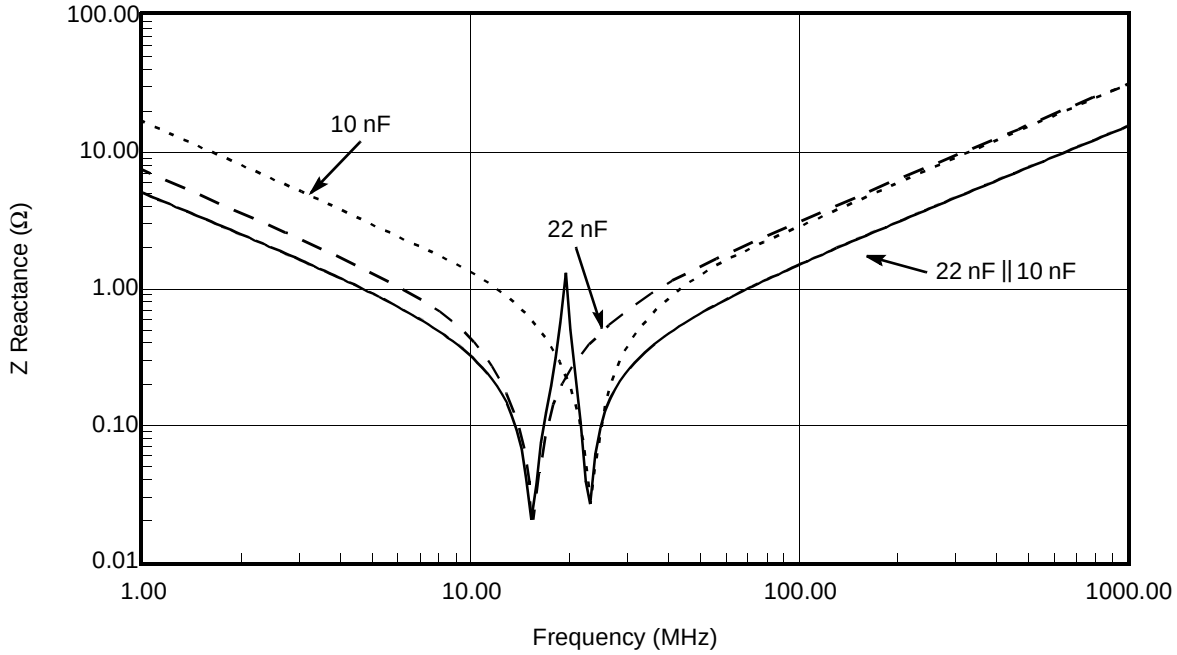

Figure 7. Real Z vs. f for Parallel 22-nF and 10-nF Capacitors

What About Multiple Clocks?

When the design calls for multiple clock frequencies, use the same raised power plane structures as shown in *Figure 6,* and use the correct value of capacitor for each section, maintaining only one value per section. Other forms of power supply isolation may be found in the Cypress application note "HOTLink Design Considerations," in the discussion on Power Distribution Requirements for Optical Drivers. The isolation provided by the slotted power plane keeps the noise of one section away from the sensitive parts of the other sections, and allows the separation of the capacitor values.

What About Variable Clock Frequencies?

Bypassing ICs when the clock rate changes over a wide range of frequencies presents the most difficult situation covered here. Fortunately, most data communications applications use only a single clock rate.

When the range of operation of a single design covers a large range of frequencies, placing two capacitors that are within approximately 2:1 of each other in capacitance results in a wider low-impedance zone and allows a broad range of bypass frequencies. Notice in *Figure 7* that the peak in the reactance still occurs, but that the maximum impedance stays well below 1.5Ω and that the usable range (less than 1.5Ω) now extends from approximately 3.25 MHz to 100 MHz. Use this multiple decoupling capacitor method only when a wide range of frequencies must be bypassed around a *single* integrated circuit and adequate range cannot be achieved by a single capacitor. Again, the capacitors must remain within a 2:1 range to prevent the reactance peak from exceeding useful limits.

Conclusions

Application of these techniques resulted in improving the measured optical margin of a HOTLink-based OLC (optical link card) by about 1 dB. It simplifies the Bill of Materials by using only one value instead of two. Finally, using only one value of capacitor provided the best jitter measurements of the HOTLink Transmitter.

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